

## **REMARKS**

Claims 1-36 remain pending in the application. Reconsideration is respectfully requested in light of the following remarks.

### **Section 103(a) Rejection:**

The Final Action rejected claims 1, 4-6, 9-12, 16, 20, 23, 26, 27, 30, 33 and 34 under 35 U.S.C. § 103(a) as being unpatentable over Fossum et al. (U.S. Patent 4,888,679) (hereinafter, "Fossum") in view of Sollars (U.S. Patent 6,216,218) (hereinafter, "Sollars"), claims 2, 19 and 21 as being unpatentable over Fossum in view of Sollars, and further in view of McClure (U.S. Patent 5,590,307), claims 3 and 22 as being unpatentable over Fossum in view of Sollars, and further in view of Faraboschi, et al. (U.S. Patent 6,122,708) (hereinafter, "Faraboschi"), claims 7, 8, 24 and 25 as being unpatentable over Fossum in view of Sollars, and in further view of Handy ("The Cache Memory Book: The Authoritative Reference on Cache Design," Academic Press, 1993, page 57), claims 13-15 and 28-29 as being unpatentable over Fossum in view of Sollars, and further in view of Microsoft ("Microsoft Computer Dictionary," Microsoft Press, 2002, page 391: parity), claims 17, 18, 31 and 32 as being unpatentable over Fossum in view of Sollars, and further in view of Morton (U.S. Patent 6,088,783), and claims 35 and 36 as being unpatentable over Fossum in view of Sollars and Morton, and further in view of Microsoft. Applicants traverse these rejections and submit that claims 1-36 are distinguishable over the cited art, as set forth in greater detail below.

Applicants submit that the cited art fails to teach or suggest all of the limitations of Applicants' claim 1. In particular, the cited art fails to teach or suggest a cache accumulator memory coupled to a memory and a functional unit, wherein the cache accumulator memory comprises a plurality of block storage locations, wherein the cache accumulator memory is configured to receive a set of one or more instructions to perform a first accumulation operation, wherein a first instruction in the set uses a first address in the memory to identify a first block operand; wherein the cache accumulator memory is

configured to accumulate an intermediate result of the first accumulation operation, wherein the intermediate result is both a result of and an operand of the first accumulation operation; and wherein in response to receiving the first instruction in the set, the cache accumulator memory is configured to access an associativity list comprising an indication that a first set of the block storage locations is allocated to the first accumulation operation and, in response to the indication, to provide the first block operand to the functional unit from the first set of block storage locations and to store the block result generated by the functional unit into the first set of block storage locations.

In the Final Action, the Examiner argues that while Fossum does not explicitly state that a cache memory is configured to accumulate an intermediate result that is both a result and an operand, such behavior is “exactly the intended purpose of a cache memory,” in that caches “store data that is needed currently, or soon to be needed... [and] thus intermediate results will certainly be accumulated and stored in the cache memory.” Applicants strongly disagree with the Examiner’s interpretation of Fossum in view of the specific language of Applicants’ claim. That a cache may be configured to store data that is produced by one operation and utilized by another operation is not in any way suggestive of a cache accumulator memory that is configured to accumulate an intermediate result of an accumulation operation, where the intermediate result is both a result of and an operand of the accumulation operation. The Examiner seems to suggest that storing data in a cache is equivalent to an accumulation operation. However, Applicants have recited a specific relationship between the result of an accumulation operation and an operand of the accumulation operation that is not in any way inherent in the data storage operation of a cache as a cache is conventionally understood or disclosed by Fossum.

Additionally, neither Fossum nor Sollars teaches or suggests that a cache accumulator memory is configured to access an associativity list comprising an indication that a first set of the block storage locations is allocated to a first accumulation operation, and that the cache accumulator memory is further configured to responsively provide a first block operand to the functional unit and to store the block result generated by the

functional unit into the first set of block storage locations. The Examiner relies upon Fossum, col. 4, lines 25-47 to teach this limitation. However, the cited portion of Fossum merely describes the general behavior of a cache in determining whether a data block is resident within the cache, and if not, fetching the data block from a main memory for storage within the cache. This is in no way suggestive of the associativity list recited in Applicants' claim.

Fossum describes the structure of the cache in further detail in col. 6, lines 20-63 and FIG. 2. However, Fossum discloses only that a cache may include a tag store 32 in conjunction with a data store 33, wherein the tag store 32 stores address bits ("tag bits") associated with data blocks stored within the data store 33, which tag bits are used as the basis for determining whether a given data block is resident within the cache. Fossum's tag bits are in no way suggestive of an associativity list that includes an indication that a set of block storage locations is allocated to a particular accumulation operation. In fact, Fossum's tag bits are not indicative of any type of association between a data block and an operation. Instead, they merely identify the data block itself for the purpose of determining a block's presence or absence within the cache.

Sollars also fails to teach or suggest an associativity list as recited in Applicants' claim. Thus, for at least the foregoing reasons, Applicants submit that claim 1 is patentably distinguishable over the cited art, as are independent claims 20, 33 and 34 having limitations similar to claim 1.

Applicants note that many of the dependent claims recite additional distinctions over the cited art. However, as the independent claims have been shown above to be distinguishable, further discussion of the dependent claims is unnecessary at the present time.

## CONCLUSION

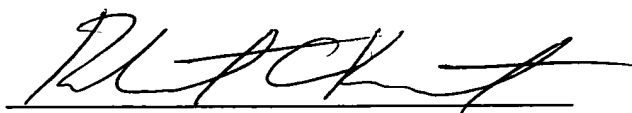
Applicants submit the application is in condition for allowance, and notice to that effect is respectfully requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5681-05300/RCK.

Also enclosed herewith are the following items:

- ☒ Return Receipt Postcard
- ☐ Petition for Extension of Time
- ☐ Notice of Change of Address
- ☐ Fee Authorization Form authorizing a deposit account debit in the amount of \$  
for fees (        ).
- ☐ Other:

Respectfully submitted,



Robert C. Kowert  
Reg. No. 39,255  
ATTORNEY FOR APPLICANT(S)

Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C.  
P.O. Box 398  
Austin, TX 78767-0398  
Phone: (512) 853-8850

Date: May 26, 2005